NW0505x Gate Driver Series

28 V, +5/-7 A, single/dual-channel gate drivers for Si/SiC MOSFETs, IGBTs, GaN HEMTs

1 Features

- Advanced SOI technology for high performance and excellent reliability
- Single/dual channel gate driver ICs to drive Si and Si/SiC MOSFETs, IGBTs, GaN HEMTs
- V_{DD} maximum rating up to 28 V
- Wide V_{DD} range from 4.8 V to 25 V
- 7 A sink and 5 A source output current enable fast switching and high efficiency
- Internal 0.8-Ω pullup and pulldown resistance
- 3.3 V, 5 V and 15 V input logic compatible
- TTL/CMOS compatible inputs
- Inputs able to sustain max V_{DD}
- Small propagation delay time (15 ns typical)
- Undervoltage Lockout (UVLO)
- Separate sink and source outputs for easy gate driving (NW0505M1S-T1 and NW0505G1S-T1)
- Output in phase with input
- Small form factor package (SOT23, SOP8)

NW0505x Gate Driver Series

Part Nr.	Channel	UVLO	Package
NW0505M1S-T1	1	4.5 V	SOT23-6
NW0505M1S-T2	1	4.5 V	SOT23-5
NW0505M1D-C1	2	4.5 V	SOP8
NW0505G1D-C1	2	10 V	SOP8

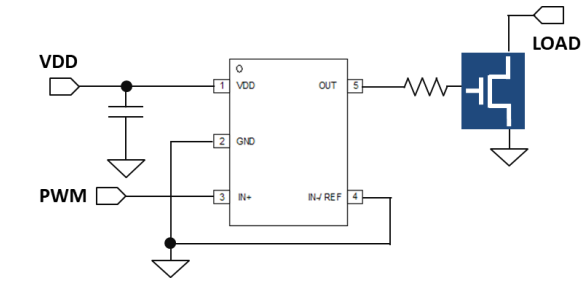
2 Description

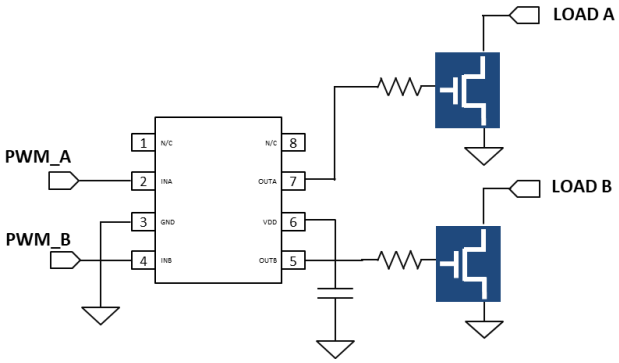
The NW0505x are a series of gate driver ICs based on advanced SOI technology, including single- and dual channel high-frequency driver ICs specialized to drive Si/SiC MOSFETs, IGBTs, GaN HEMTs, along with various packages and UVLO voltage options.

The NW0505x gate drivers provide 5 A source and 7 A sink peak currents with small propagation delay.

3 Application

- Switch-Mode Power Supplies (SMPS)
- PFC Systems
- DC/DC Power Converters
- Power Conversion Systems (PCS)
- Energy Storage Systems
- Solar Micro-Inverters
- Solar Optimizers





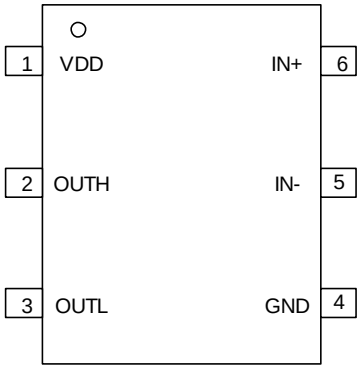
4 Table of Contents

5 Pin Configuration and Functions

5.1 NW0505M1S-T1

SOT23-6 Package

(Top view)



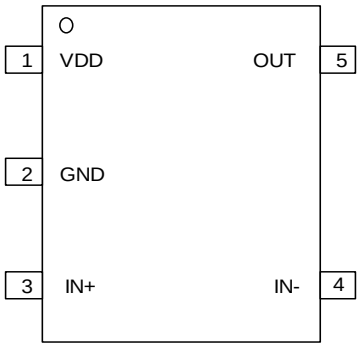
PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VDD	1	P	Power supply
OUTH	2	O	Driver sourcing current output
OUTL	3	O	Driver sinking current output
GND	4	P	Ground
IN-	5	I	Inverting input. Connect IN- to GND in noninverting input configuration
IN+	6	I	Noninverting input. Connect IN- to V_{DD} in inverting input configuration

[1] I = Input, O = Output, P = Power, NC = Not Connected

5.2 NW0505M1S-T2

SOT23-5 Package

(Top view)



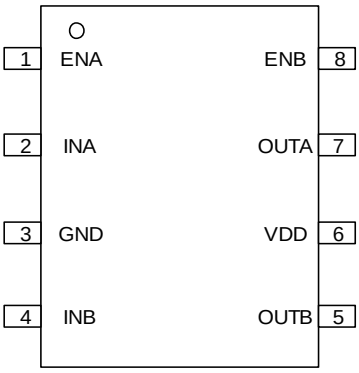
PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD	1	P	Power supply
GND	2	P	Ground
IN+	3	I	Noninverting input. Connect IN- to V_{DD} in inverting input configuration
IN-	4	I	Inverting input. Connect IN- to GND in noninverting input configuration
OUT	5	O	Driver output

(1) I = Input, O = Output, P = Power, NC = Not Connected

5.3 NW0505M1D-C1 & NW0505G1D-C1

SOP8 Package

(Top view)



PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable input of channel A. if ENA is high or left open, OUTA is controlled by INA. If ENA is low, OUTA is low regardless of INA.
INA	2	I	Noninverting input of channel A
GND	3	P	Ground
INB	4	I	Noninverting input of channel B
OUTB	5	O	Driver output of channel B
VDD	6	P	Power supply
OUTA	7	O	Driver output of channel A
ENB	8	I	Enable input of channel B. if ENB is high or left open, OUTB is controlled by INB. If ENB is low, OUTB is low regardless of INB.

(1) I = Input, O = Output, P = Power, NC = Not Connected

6 Specifications

6.1 Absolute maximum ratings

Parameter		Values	Unit
V_{DD}	Supply Voltage	28	V
IN+/IN-/INA/INB	Input Voltage	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{DD} + 0.3	V
T_J	Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-55 to +150	°C
ENA/ENB	Voltage of enable pin	-0.3 to V_{DD} + 0.3	V

6.2 ESD Rating

Parameter		Values	Unit
ESD	HBM	±1000	V
	CDM	±500	V

6.3 Thermal Information

Parameter		Values			Unit
		SOT23-5	SOT23-6	SOP8	
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance	220	220	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case Thermal Resistance	100	100	70	°C/W

6.4 Recommended Operating Conditions

Parameter		MIN	NOM	MAX	Unit
V_{DD}	Supply Voltage	4.8	12	25	V
PWM	PWM Input Voltage	0	5	V_{DD}	V
T_J	Operating Junction Temperature	-40	25	125	°C

6.5 Electrical Characteristics

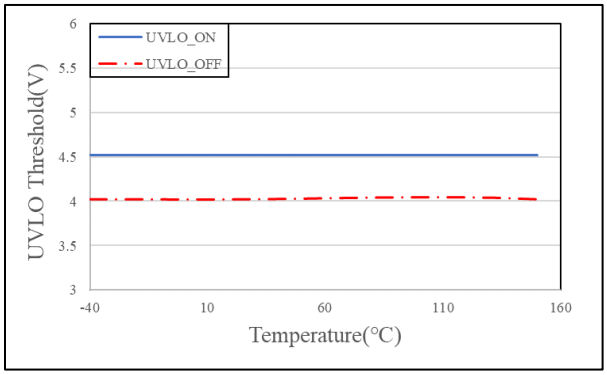
V_{DD}=12V, T_j= -40°C to 125 °C unless otherwise noted.

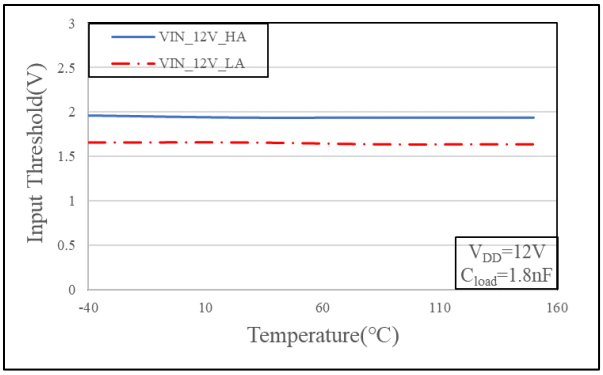
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
SUPPLY CURRENTS						
I_{QC}	V_{DD} quiescent current	0.76	1.08	1.40	mA	V_{IN} = 0V, V_{DD} = 12 V
UNDER-VOLTAGE LOCKOUT (UVLO)						
$V_{UVLO4.8+}$	UVLO 4.8 V turn-on Threshold (3)	4.3	4.5	4.8	V	
$V_{UVLO4.8-}$	UVLO 4.8 V turn-off Threshold (3)	3.5	4.0	4.2	V	
$V_{UVLO4.8H}$	UVLO 4.8 V Hysteresis (3)	-	0.48	-	V	
$V_{UVLO12+}$	UVLO 12 V turn-on Threshold (4)	9.5	10	10.5	V	
$V_{UVLO12-}$	UVLO 12 V turn-off Threshold (4)	8.5	9	9.5	V	
$V_{UVLO12H}$	UVLO 12V Hysteresis (4)	-	1	-	V	
(3) NW0505M1S-T1, NW0505M1S-T2, NW0505M1D-C1 (4) NW0505G1D-C1						
GATE DRIVER						
I_{O+}	Peak sourcing output current	-	5	-	A	C = 100 nF, V_{DD} = 16 V
I_{O-}	Peak sinking output current	-	7	-	A	C = 100 nF, V_{DD} = 16 V
R_{GH}	Turn-on internal gate resistance	-	700	-	mΩ	V_{IN} = 5 V, I_{LO} = 500 mA
R_{GL}	Turn-off internal gate resistance	-	500	-	mΩ	V_{IN} = 0V, I_{LO} = -500 mA
INPUTS (IN+, IN-, ENA, ENB)						
V_{IN_H}	Input signal high Threshold	1.7	1.9	2	V	
V_{IN_L}	Input signal low Threshold	1.4	1.6	1.8	V	
V_{IN_Hyst}	Input signal Hysteresis	-	0.2	-	V	
R_{IN_H}	Input pull-up resistor IN- (1)	-	400	-	KΩ	
R_{IN_L}	Input pull-down resistor IN+ (2)	-	300	-	KΩ	
(1) Inputs with initial high logic level (2) Inputs with initial low logic level						

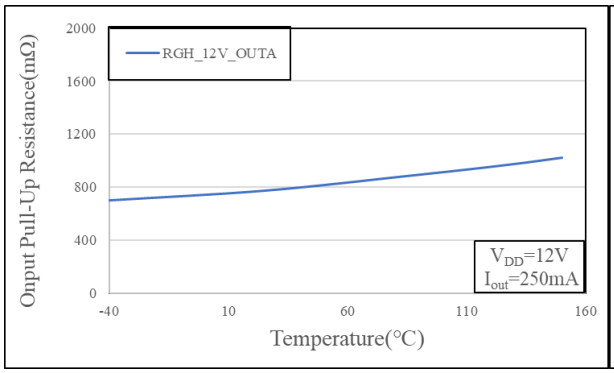
6.6 Switching Characteristics

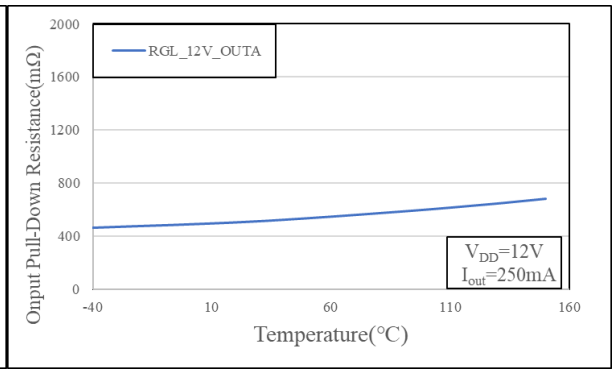
Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
SWITCHING CHARACTERISTICS						
t_{ON}	Turn-on propagation delay	-	15	-	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12 V, from 50% to 50%
t_{OFF}	Turn-off propagation delay	-	18	-	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12 V, from 50% to 50%
t_R	Output rise time	-	2.5	-	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12V, from 10% to 90%
t_F	Output fall time	-	3.5	-	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12 V, from 10% to 90%

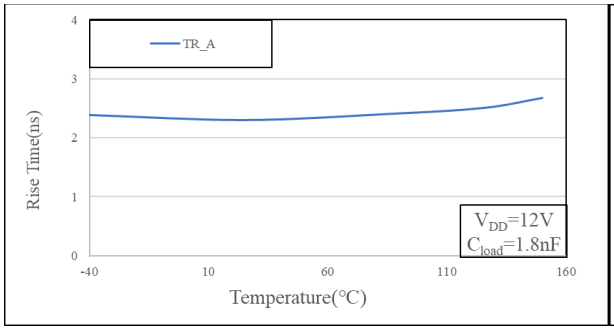
7 Plots of typical Characteristics

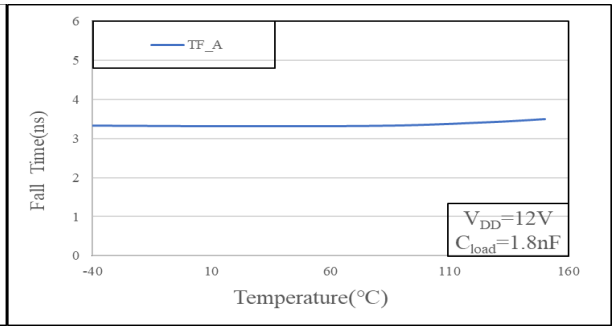


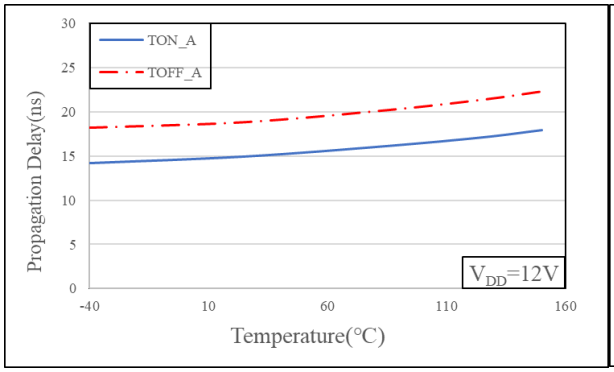


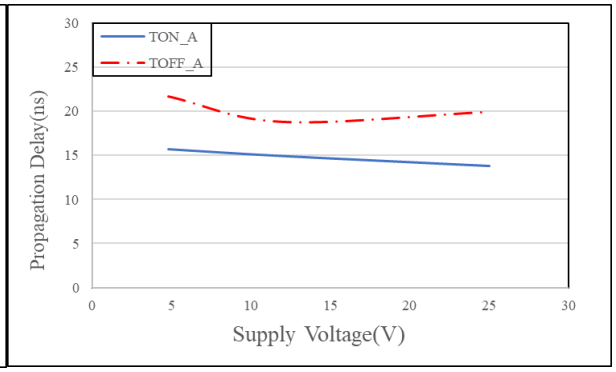


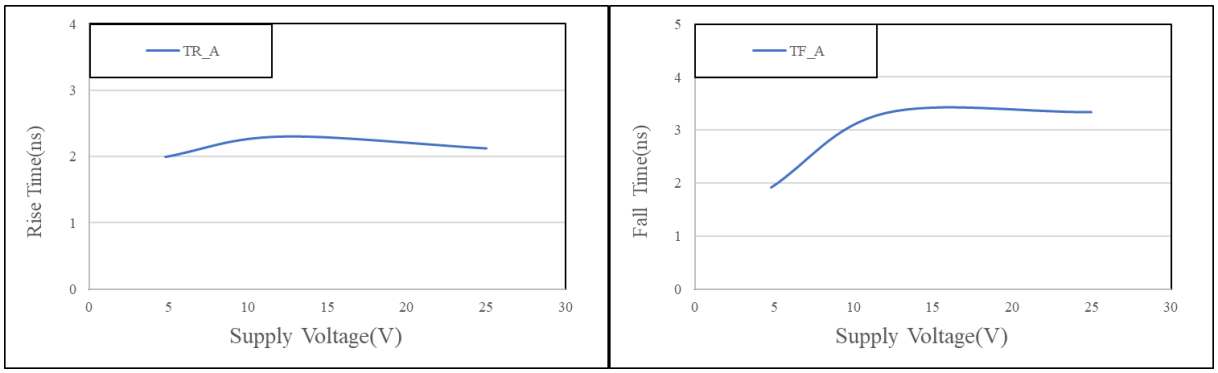












8 Functional Description

8.1 Overview

The NW0505x series gate drivers include single-channel and dual channels high-frequency gate driver ICs specialized to drive GaN HEMTs/ Si & SiC MOSFETs / IGBTs, offering multiple packages and UVLO voltage options.

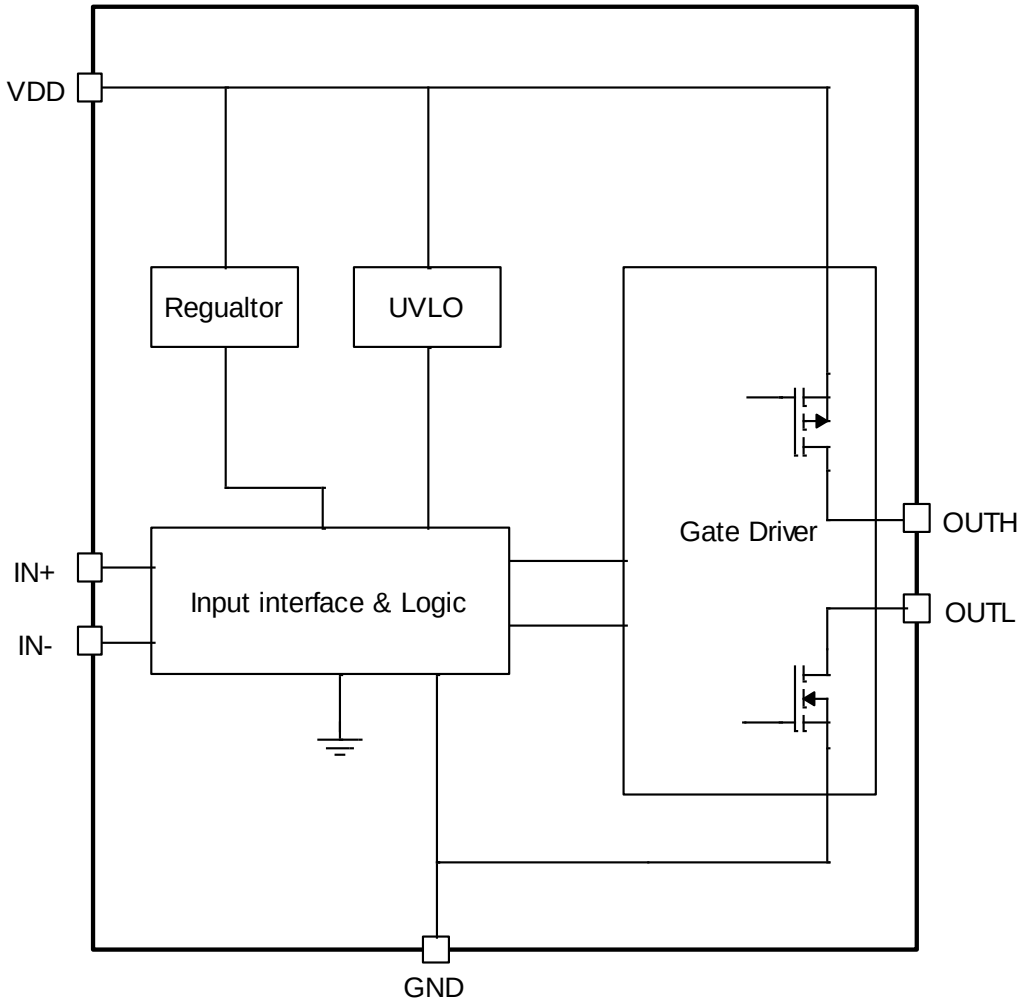
The NW0505x gate drivers provide 5 A source and 7 A sink peak current capability with small propagation delay.

The split output pins, OUTH and OUTL, allow the user to apply different turn-on and turn-off resistors and control on/off slew rate independently. The OUTH and OUTL can be tied together as single output configuration.

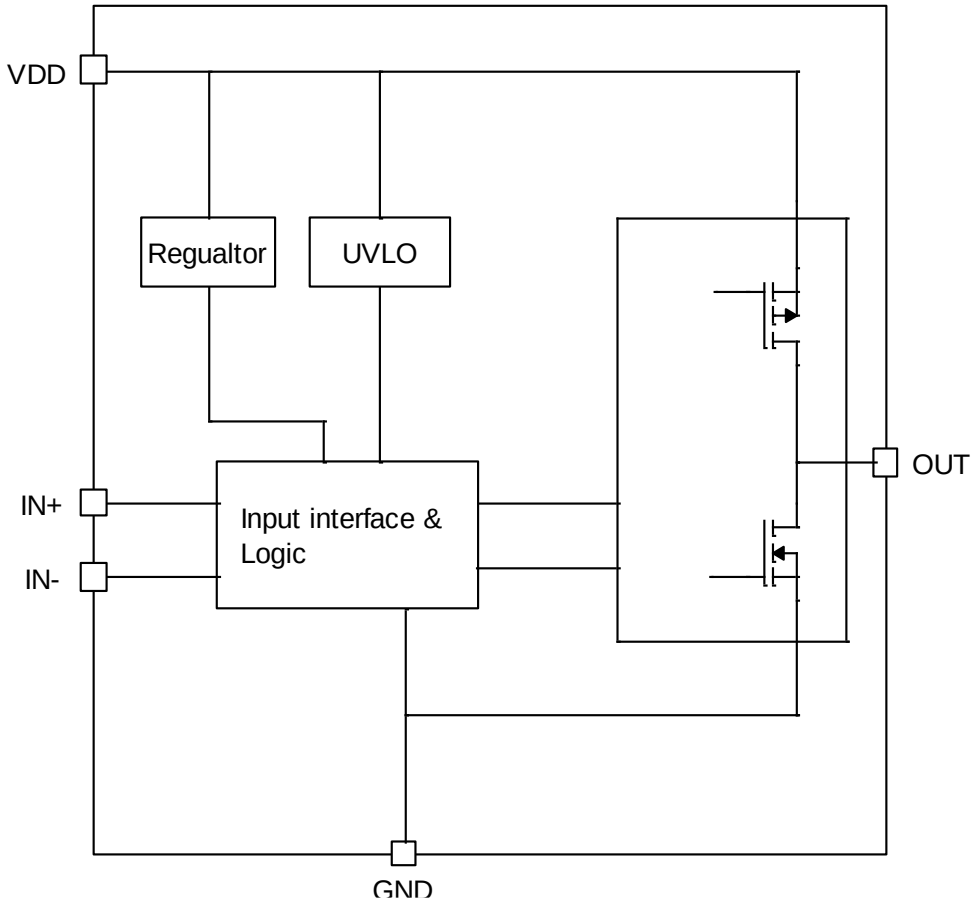
The NW0505x can operate in a wide V_{DD} range from 4.5 V to 25 V, along with internal undervoltage lockout (UVLO) designed to effectively protect the power devices.

The NW0505x supports dual input with inverting (IN-) and non-inverting (IN+) configurations. The input threshold is compatible with TTL/CMOS logics.

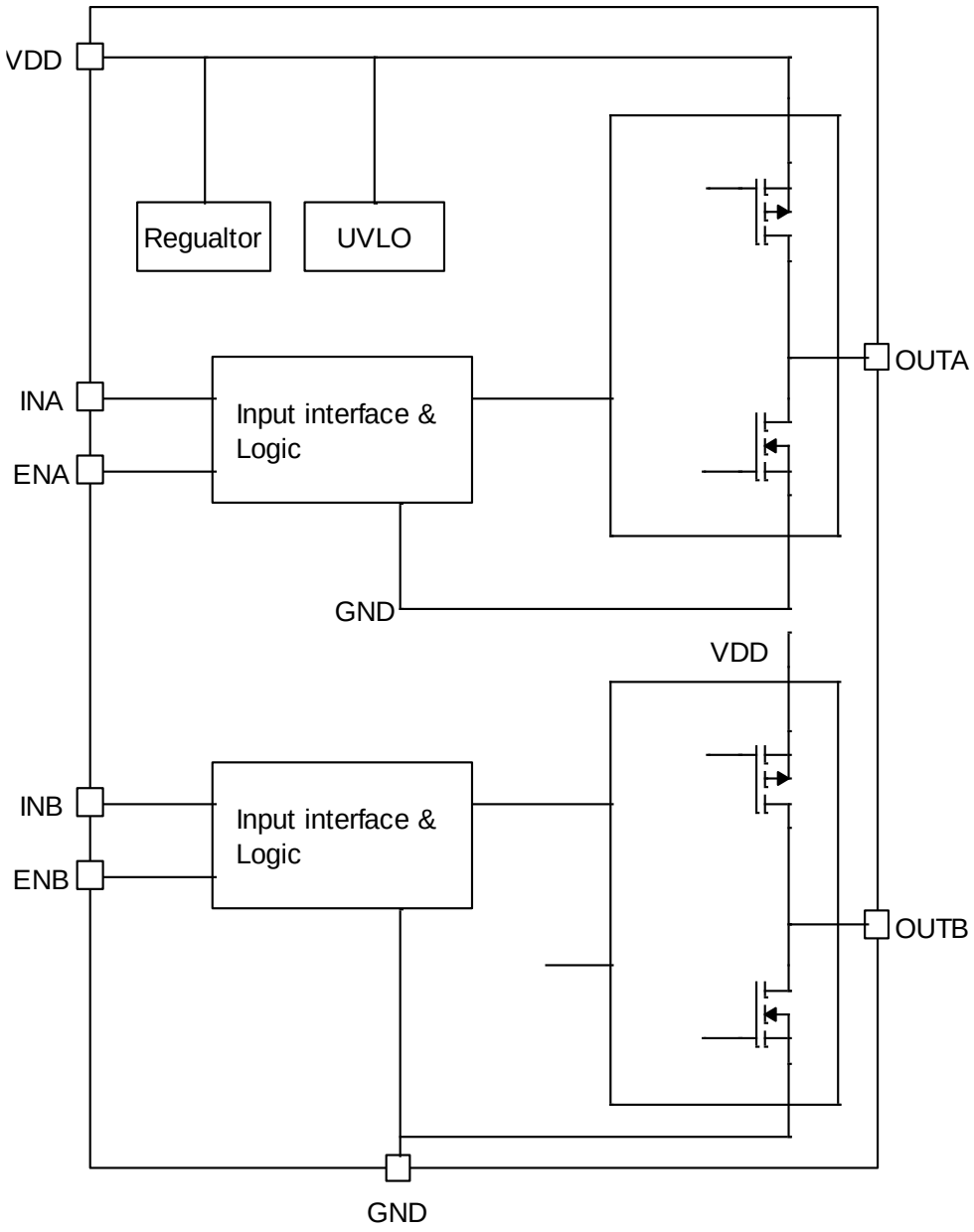
8.2 Block Diagram (NW0505M1S-T1)



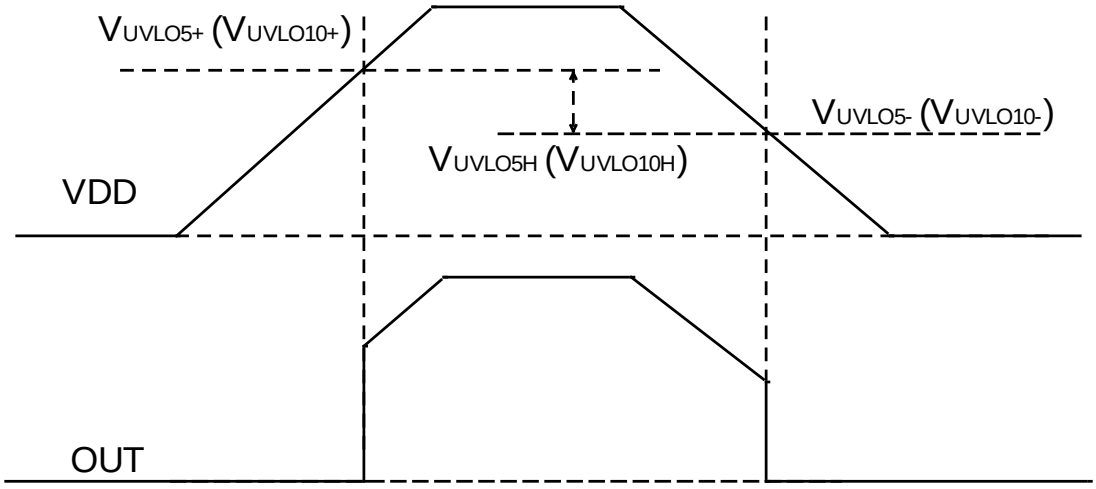
8.3 Block Diagram (NW0505M1S-T2)



8.4 Block Diagram (NW0505M1D-C1 & NW0505G1D-C1)



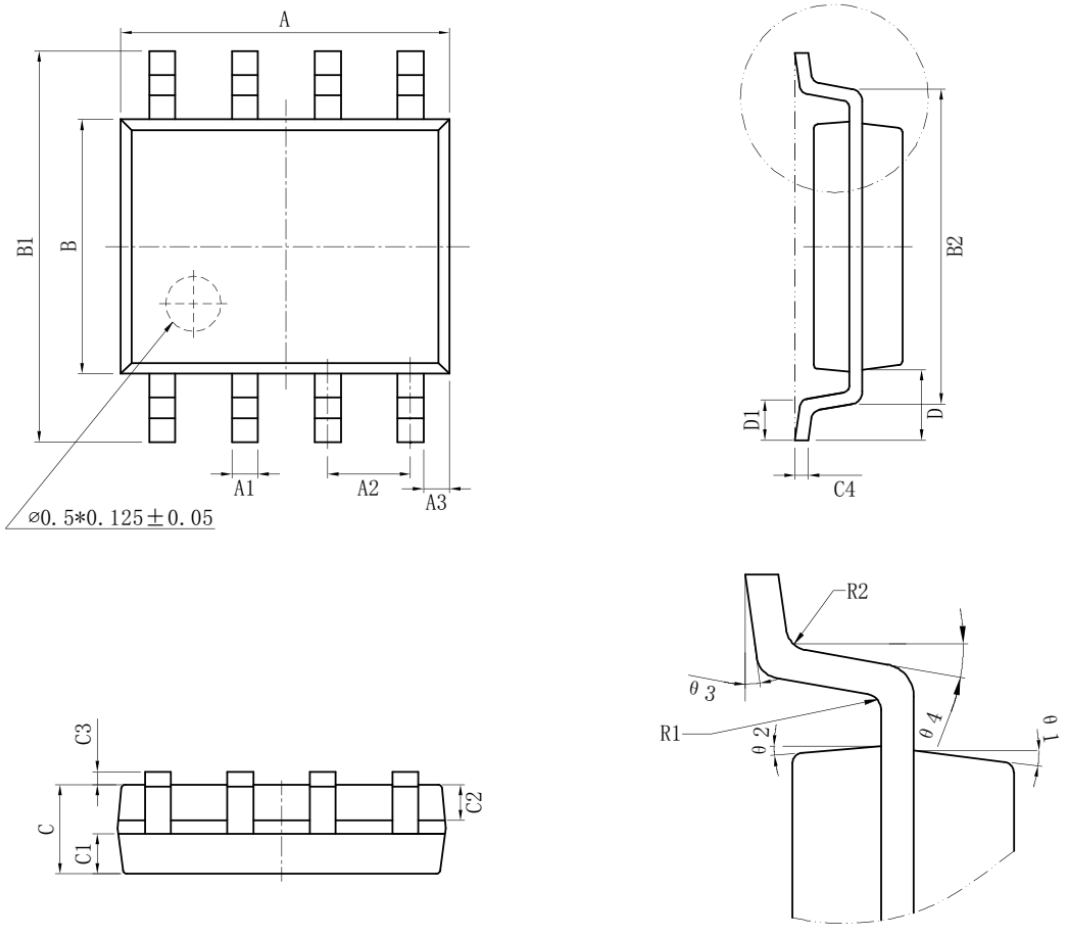
8.5 Under Voltage Lockout (UVLO)



9 Package and Bonding Information

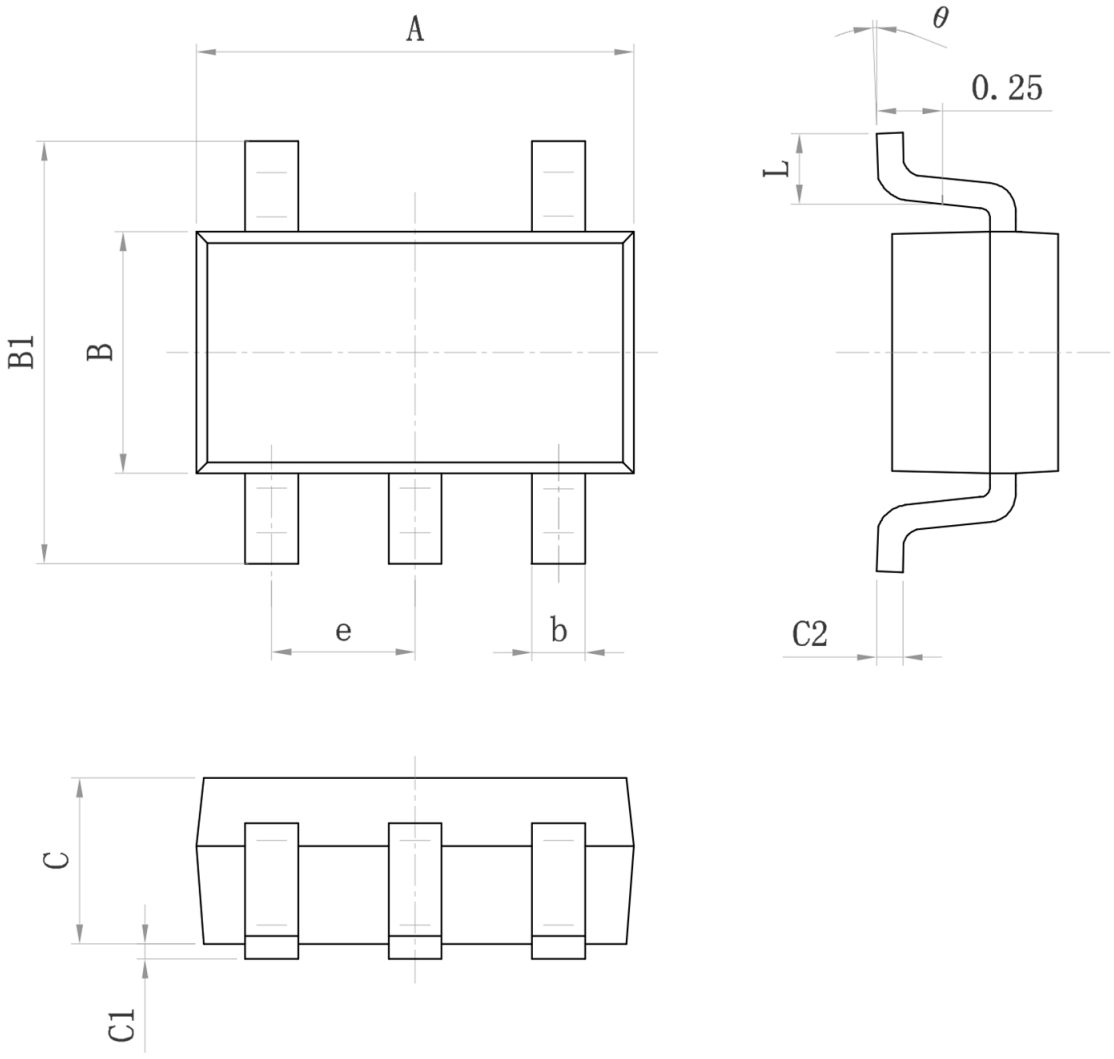
9.1 SOP8

Symbol	Dimension (mm)		Symbol	Dimension (mm)	
	Min	Max		Min	Max
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27 (typ)		D	1.05 (typ)	
A3	0.345 (typ)		D1	0.40	0.80
B	3.80	4.00	R1	0.20 (typ)	
B1	5.80	6.20	R2	0.20 (typ)	
B2	5.00 (typ)		θ1	17° (typ)	
C	1.30	1.60	θ2	13° (typ)	
C1	0.55	0.65	θ3	0°	8°
C2	0.55	0.65	θ4	4°	12°



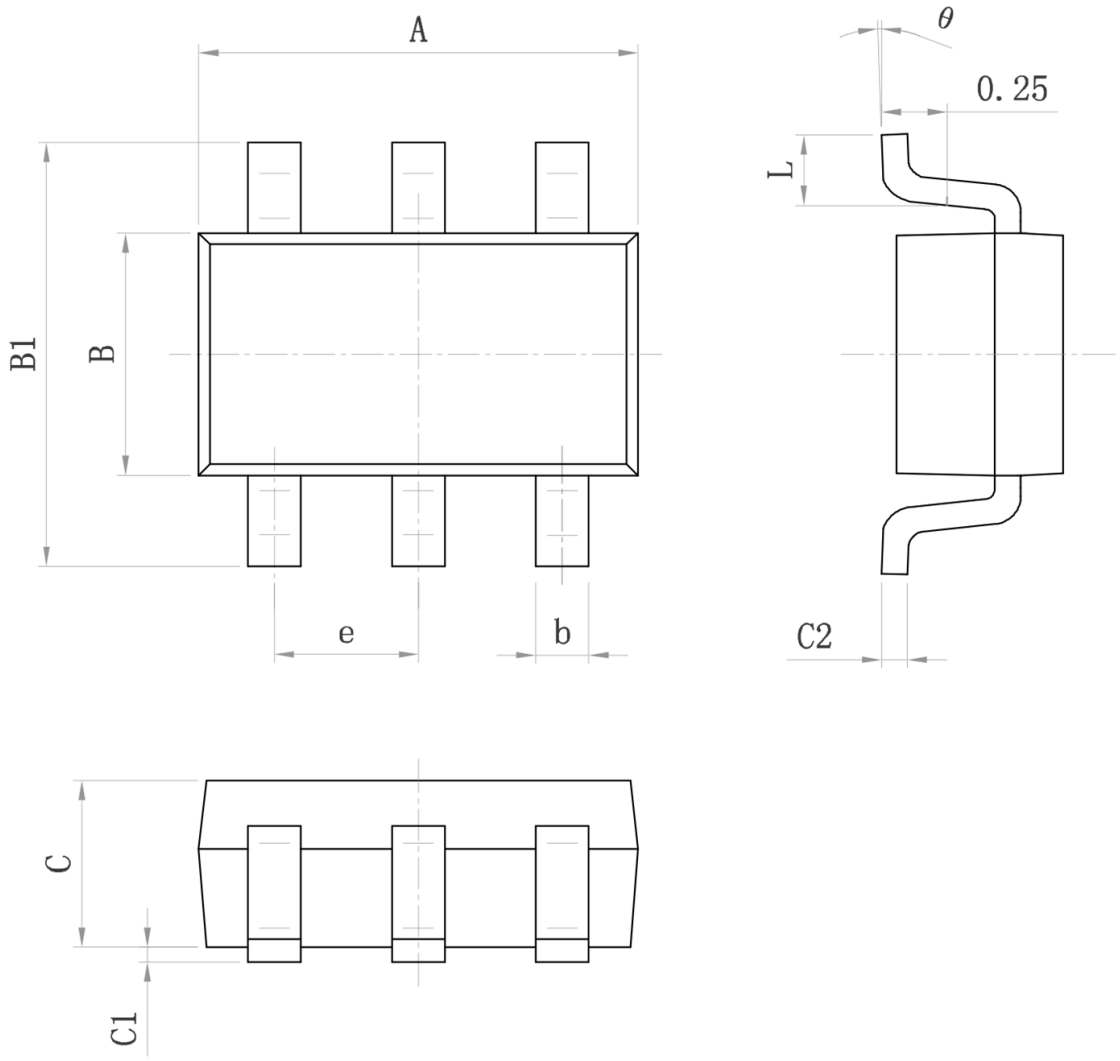
9.2 SOT23-5

Symbol	Dimension (mm)		Symbol	Dimension (mm)	
	Min	Max		Min	Max
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°



9.3 SOT23-6

Symbol	Dimension (mm)		Symbol	Dimension (mm)	
	Min	Max		Min	Max
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°



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