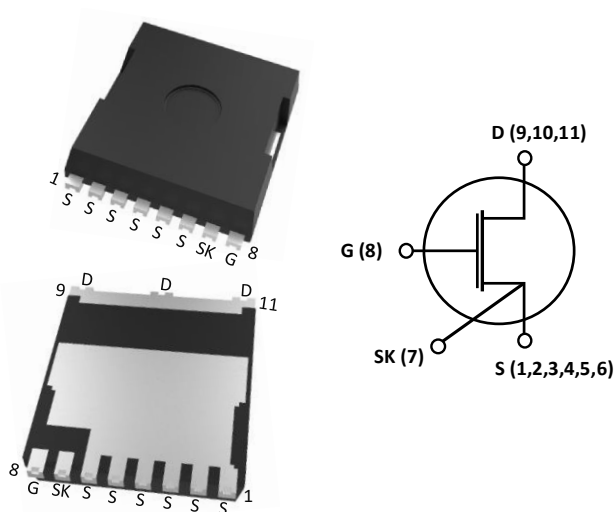


6512EL1

650 V E-mode GaN Transistor

Features

- 650 V enhancement mode GaN power transistor
- Advanced GaN-on-QST technology
- TOLL package
- Typical $R_{DS(on)} = 120\text{ m}\Omega$
- $I_{DS\ max,DC} = 12\text{ A}$
- Simple gate drive 0 V to 6 V and large $V_{GS(th)}$
- High switching frequency ($> 1\text{ MHz}$)
- Reverse conduction capability
- Zero reverse recovery loss
- Kelvin Source for optimized gate drive
- CDM 1 kV



Applications

- PD chargers
- Power Adapters
- Power Factor Correctors
- Appliance Motor Drive
- Industrial Power Supplies

Description

The 6512EL1 is an enhancement mode GaN transistor designed for large power density and high switching frequency. Its large threshold voltage and the presence of a kelvin source connection enable fast and safe gate driving. These features enable high efficiency and reliable power switching.

Pin Description

Pin No.	Pin Name	Description
9,10,11	D	Drain
1,2,3,4,5,6	S	Source
7	SK	Kelvin Source
8	G	Gate

Absolute Maximum Ratings

$T_J = 25\text{ }^\circ\text{C}$ except as noted. Exceeding the maximum ratings may damage the device.

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage – transient (Note 1)	V_{DS} (transient)	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage – transient (Note 1)	V_{GS} (transient)	-20 to 10	V
Continuous Drain Current ($T_{case} = 25\text{ }^\circ\text{C}$)	I_{DS}	12	A
Pulsed Drain Current ($T_{case} = 25\text{ }^\circ\text{C}$) (Pulse width 10us, $V_{GS} = 6\text{ V}$) (Note 2)	$I_{DS, Pulse}$	22.5	A
Pulsed Drain Current ($T_{case} = 150\text{ }^\circ\text{C}$) (Pulse width 10us, $V_{GS} = 6\text{ V}$) (Note 2)	$I_{DS, Pulse}$	12	A
Max Power Dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	P_{tot}	130	W
Operating Junction Temperature	T_J	-55 to +150	$^\circ\text{C}$
Storage Temperature Range	T_S	-55 to +150	$^\circ\text{C}$

Note 1: for pulses $\leq 100\text{us}$

Note 2: Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-to-Case – (bottom side)	$R_{TH,J-C}$	0.96	$^\circ\text{C/W}$
Thermal Resistance Junction-to-ambient (Note 3)	$R_{TH,J-A}$	34.5	$^\circ\text{C/W}$

Note 3: Based on a 4-layer, 1.6 mm-thick PCB. The copper thickness of the external layer is 2 oz. while the buried layers are 1 oz. thick. PCB in a horizontal position without air stream cooling.

Electrical Characteristics

Static Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Condition
Drain-to-Source On Resistance	$R_{DS(on)}$	-	120	168	mΩ	$I_{DS} = 3.5 \text{ A}, V_{GS} = 6 \text{ V}, T_J = 25 \text{ }^\circ\text{C}$
		-	240	-	mΩ	$I_{DS} = 3.5 \text{ A}, V_{GS} = 6 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	1.3	2	2.6	V	$I_{DS} = 1.2 \text{ mA}, T_J = 25 \text{ }^\circ\text{C}$
		-	1.7	-	V	$I_{DS} = 1.2 \text{ mA}, T_J = 150 \text{ }^\circ\text{C}$
Gate-to-Source Current	I_{GS}	-	240	-	μA	$V_{GS} = 6 \text{ V}, T_J = 25 \text{ }^\circ\text{C}$
Drain-to-Source Leakage Current	I_{DSS}	-	11	-	μA	$V_{DS} = 650 \text{ V}, T_J = 25 \text{ }^\circ\text{C}$
		-	45	-	μA	$V_{DS} = 650 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$
Internal Gate Resistance	R_G	-	0.7	-	Ω	$f = 5 \text{ MHz}, \text{ open drain}$

Dynamic Characteristics

Input Capacitance	C_{ISS}	-	153	-	pF	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, f = 100 \text{ kHz}$
Output Capacitance	C_{OSS}	-	35	-	pF	
Reverse Transfer Capacitance	C_{RSS}	-	0.3	-	pF	
Effective Output Capacitance, Energy-Related (Note 4)	$C_{O(ER)}$	-	50	-	pF	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$
Effective Output Capacitance, Time-Related (Note 5)	$C_{O(TR)}$	-	70.3	-	pF	
Output Charge	Q_{OSS}	-	28.1	-	nC	$V_{DS} = 0 \text{ V to } 400 \text{ V}$
Turn-On Delay	$t_{D(on)}$	-	2.9	-	ns	$V_{DD} = 400 \text{ V}, V_{GS} = 0 \text{ to } 6 \text{ V}, I_{DS} = 10 \text{ A}, R_{G(on)} = 10 \text{ } \Omega, R_{G(off)} = 2.2 \text{ } \Omega$ (see Figure 14,15)
Rise Time	t_R	-	6.3	-	ns	
Turn-Off Delay	$t_{D(off)}$	-	4.4	-	ns	
Fall Time	t_F	-	5	-	ns	
Switching Energy During Turn-on	E_{on}	-	21.2	-	μJ	

Switching Energy During Turn-off	E_{off}	-	7.8	-	μJ	
Output Capacitance Stored Energy	E_{OSS}	-	4	-	μJ	$V_{DS} = 0 \text{ V to } 400 \text{ V}$

Note 4: $C_{O(ER)}$ is a fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS} .

Note 5: $C_{O(TR)}$ is a fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS} .

Gate Charge Characteristics

Total Gate Charge	Q_G	-	5.65	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V},$ $V_{DS} = 0 \text{ to } 400 \text{ V},$ $I_{DS} = 5 \text{ A}$
Gate-to-Source Charge	Q_{GS}	-	0.2	-	nC	
Gate-to-Drain Charge	Q_{GD}	-	2.95	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.45	-	V	$V_{DS} = 400 \text{ V}, I_{DS} = 5 \text{ A}$

Reverse Conduction Characteristics

Source-Drain Reverse Voltage	V_{SD}	-	2.5	-	V	$V_{GS} = 0 \text{ V}, I_{SD} = 2 \text{ A}$
Reverse Recovery Charge	Q_{rr}	-	0	-	nC	
Reverse Recovery Time	t_{rr}	-	0	-	ns	

Electrostatic Discharge (ESD) Classification

Parameters	Symbol	Notes
Charge Device Model	CDM	$\geq 1 \text{ kV}$

Electrical Performance Graphs

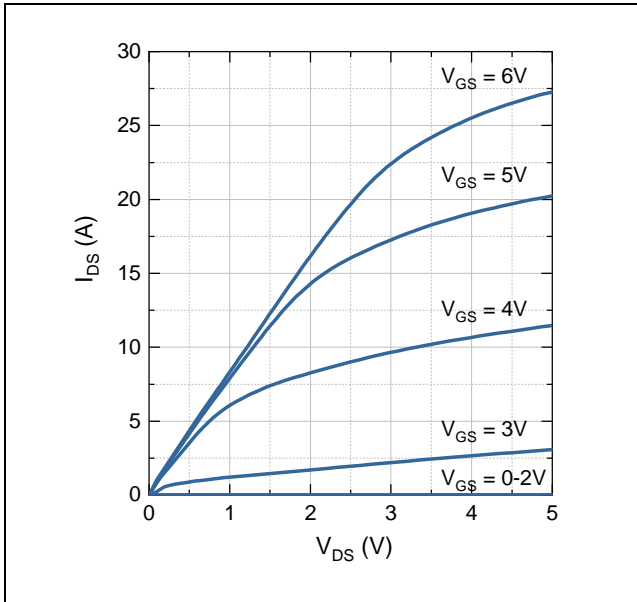


Figure 1: Typical pulsed I_{DS} vs. V_{DS} at $T_J = 25\text{ }^\circ\text{C}$

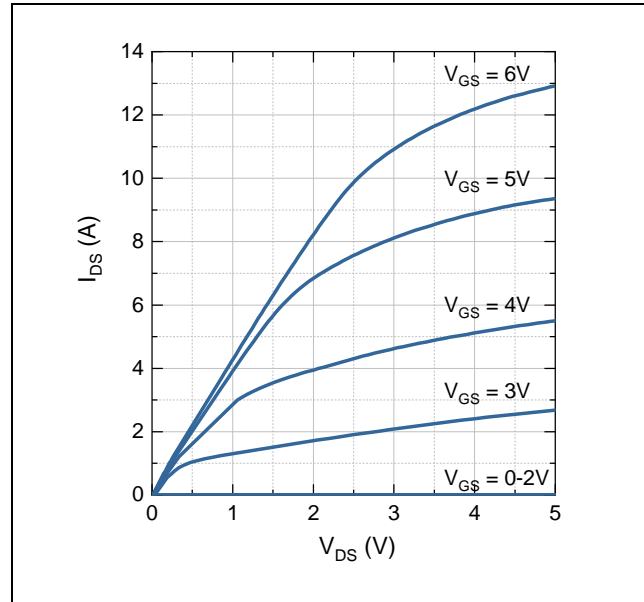


Figure 2: Typical pulsed I_{DS} vs. V_{DS} at $T_J = 150\text{ }^\circ\text{C}$

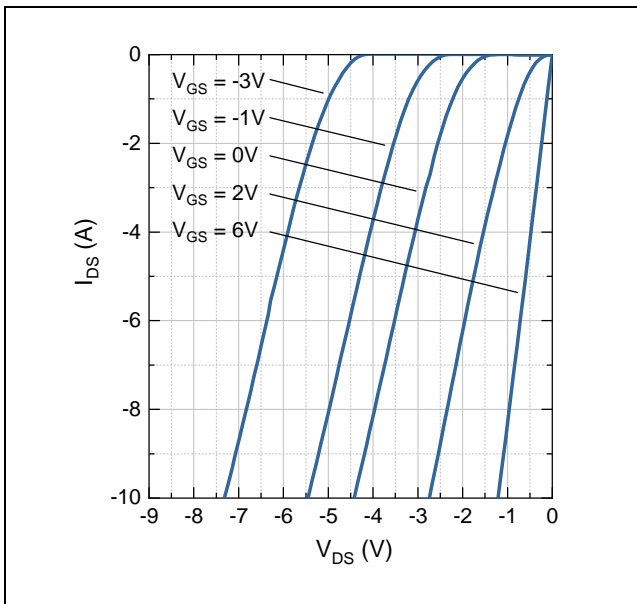


Figure 3: Typical Reverse Conduction Characteristics at $T_J = 25\text{ }^\circ\text{C}$

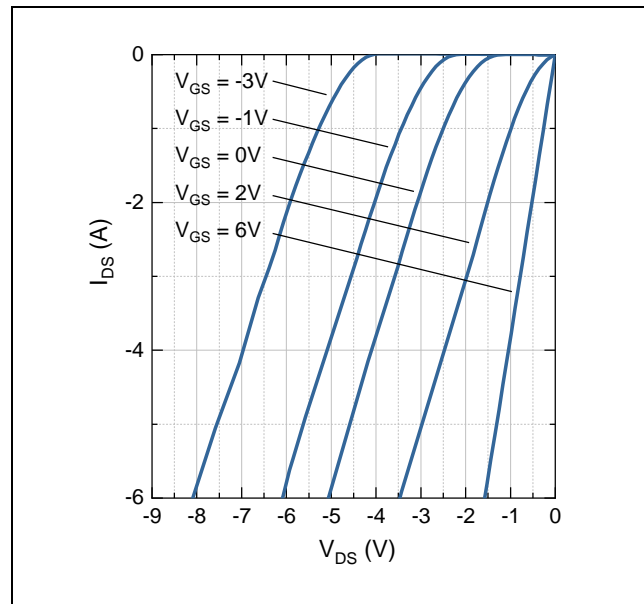


Figure 4: Typical Reverse Conduction Characteristics at $T_J = 150\text{ }^\circ\text{C}$

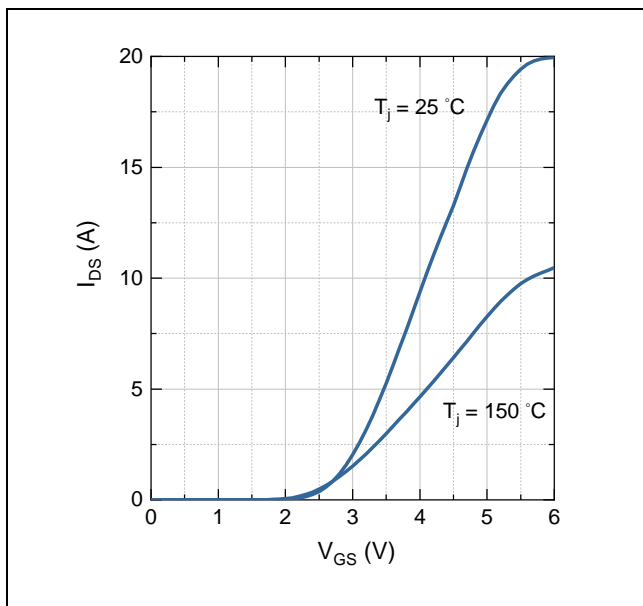


Figure 5: Typical I_{DS} vs. V_{GS} at $T_j = 25\text{ °C}$ and $T_j = 150\text{ °C}$ for $V_{DS} = 3\text{ V}$

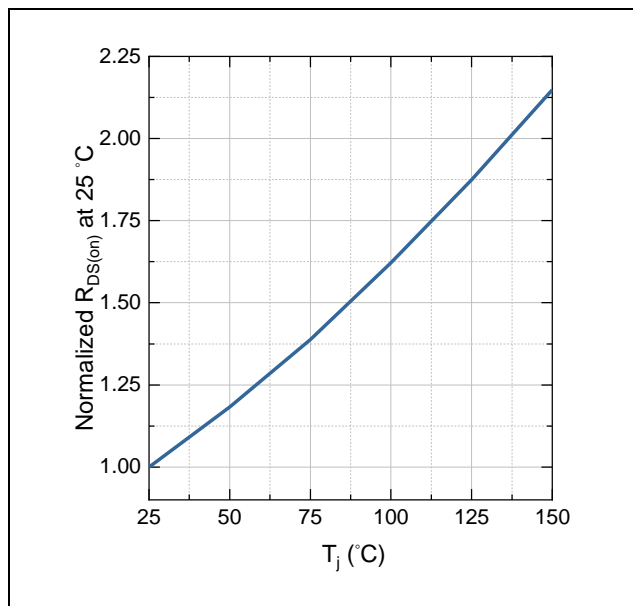


Figure 6: Normalized $R_{DS(on)}$ as a function of T_j

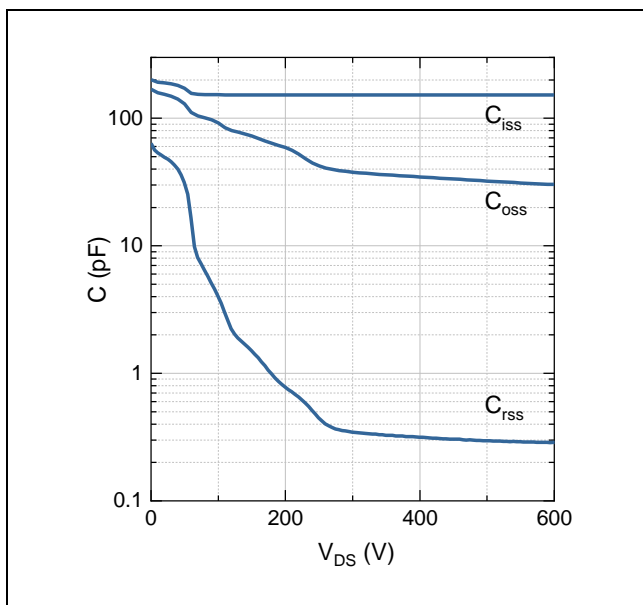


Figure 7: Typical C_{ISS} , C_{OSS} , C_{RSS} vs. V_{DS}

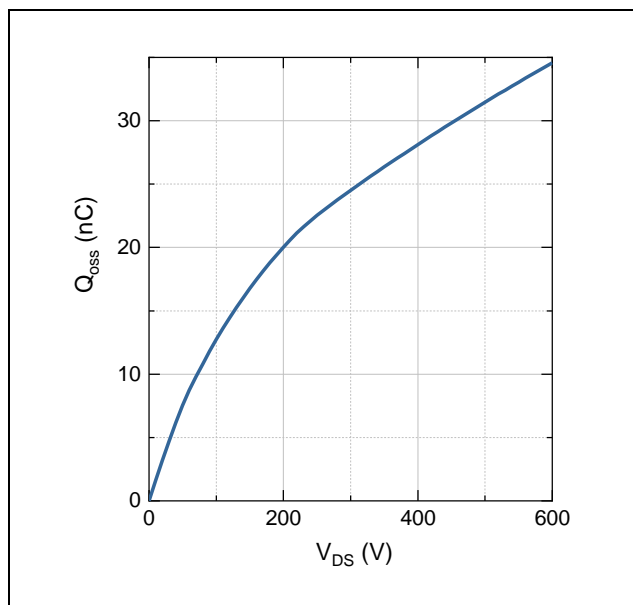


Figure 8: Typical charge stored in C_{OSS}

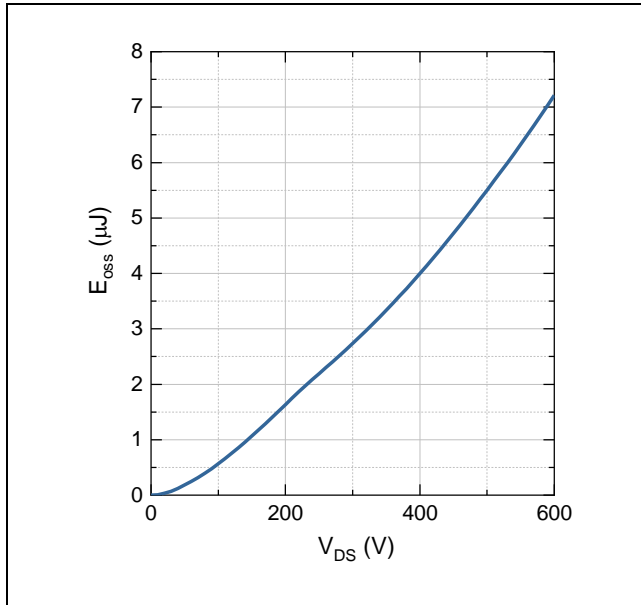


Figure 9: Typical energy stored in C_{oss}

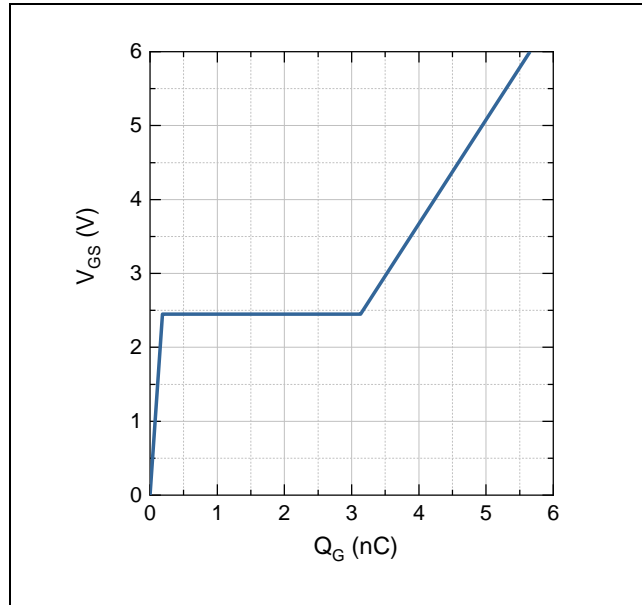


Figure 10: Typical V_{GS} vs. Q_G at V_{DS} = 400 V

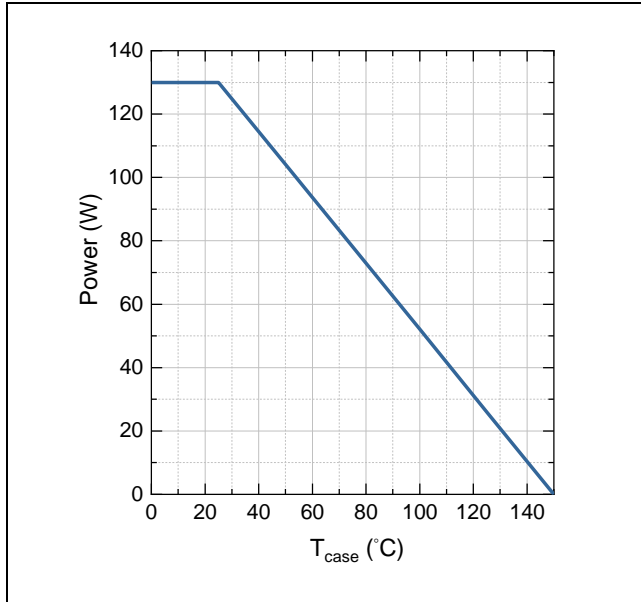


Figure 11: Power Derating vs. T_{case}

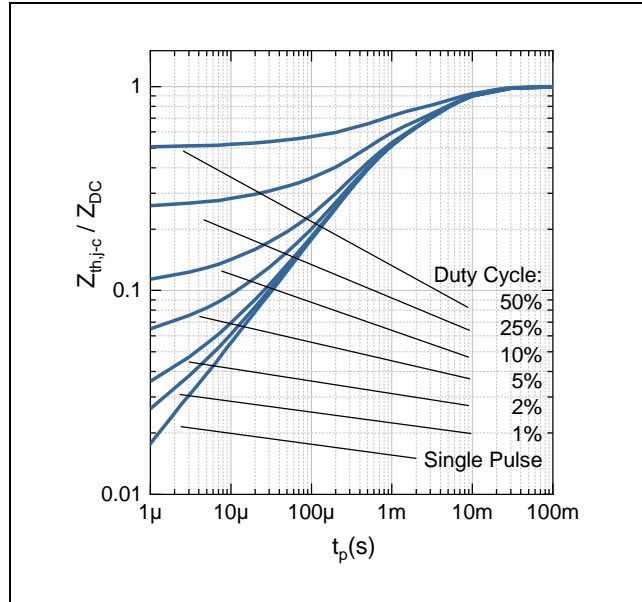


Figure 12: Transient Thermal Impedance

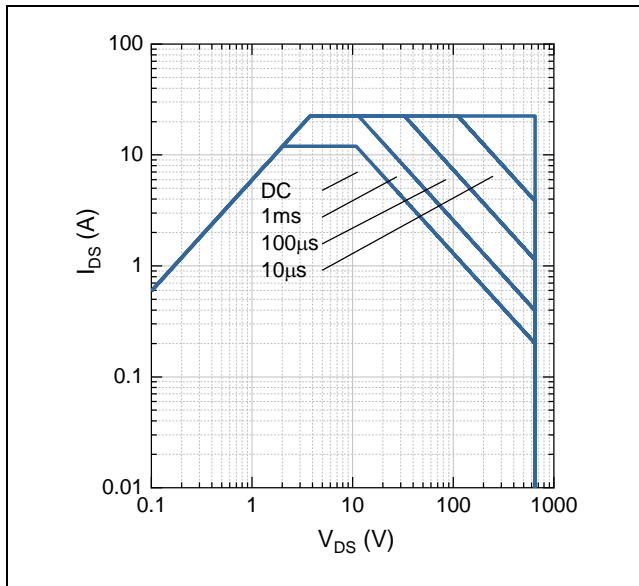


Figure 13: Safe Operating Area at $T_{case} = 25\text{ }^{\circ}\text{C}$

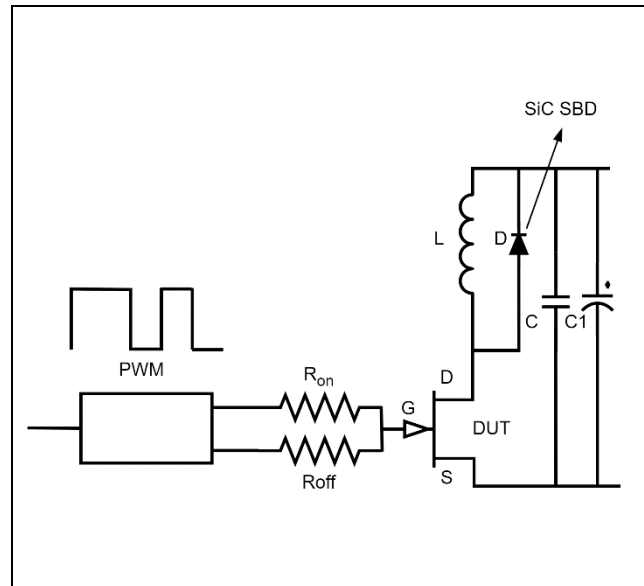


Figure 14: DPT circuit used for switching times measurement, $V_{DS} = 400\text{ V}$, $I_{DS} = 10\text{ A}$, $L = 400\text{ }\mu\text{H}$, $V_{GS} = 6\text{ V}$, $R_{on} = 10\text{ }\Omega$, $R_{off} = 2.2\text{ }\Omega$

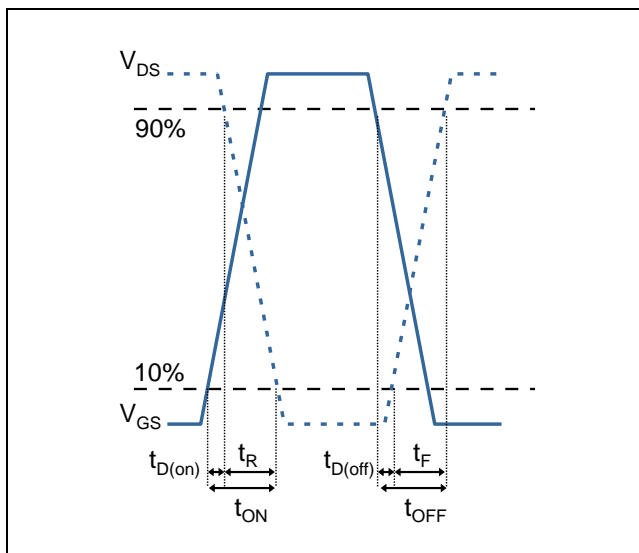
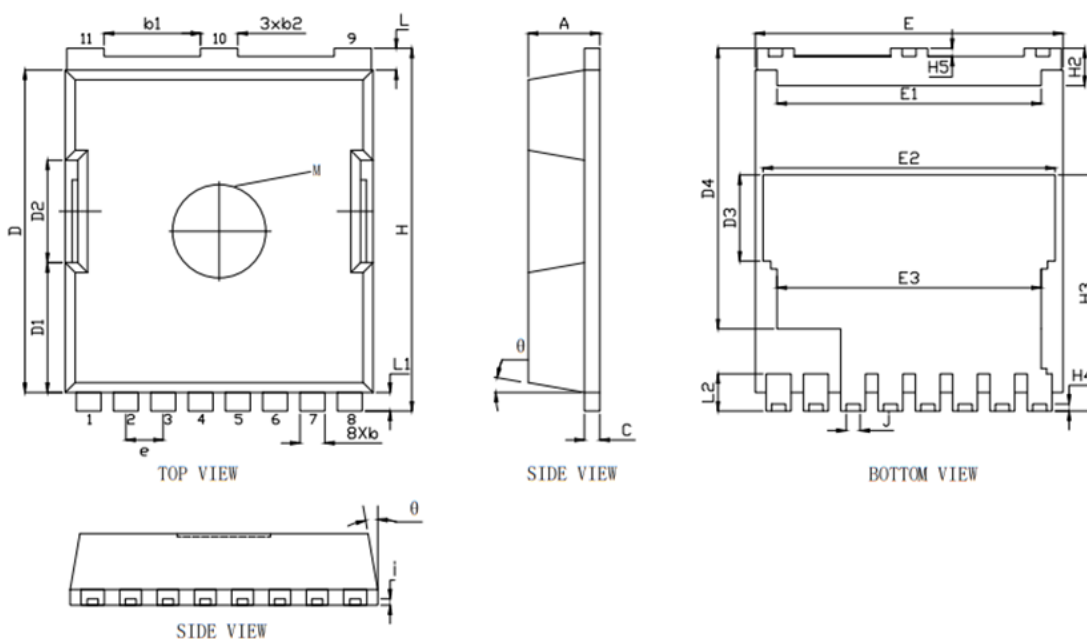


Figure 15: Switching waveform used to determine the switching times values

Package Information



SYMBLE	MILLIMETER			SYMBLE	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	2.20	2.30	2.40	e	1.10	1.20	1.30
b	0.70	0.80	0.90	H	11.48	11.68	11.88
b1	3.00	3.10	3.20	H2	1.00	1.20	1.40
b2	1.10	1.20	1.30	H3	7.50	7.60	7.70
c	0.40	0.50	0.60	H4	0.13	0.23	0.33
D	10.18	10.38	10.58	H5	0.26 REF		
D1	4.18 REF			i	0.10	-	-
D2	3.30 REF			j	0.42	0.45	0.50
D3	2.77 REF			L	0.50	0.70	0.90
D4	9.03 REF			L1	0.50	0.60	0.70
E	9.70	9.90	10.10	L2	1.05	1.20	1.30
E1	8.50 REF			M	3 REF		
E2	9.40 REF			θ	8°	10°	12°
E3	8.50 REF						

Notes:

- (1) Dimension and tolerance conform to ASME Y14.5-2009.
- (2) All dimensions are in millimeters.
- (3) Lead coplanarity shall be 0.1 millimeters max.
- (4) Complies with JEDEC MO-229.
- (5) Drawing is not to scale.
- (6) Dimensions do not include mold protrusion.
- (7) Package outline exclusive of metal burr dimensions.

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