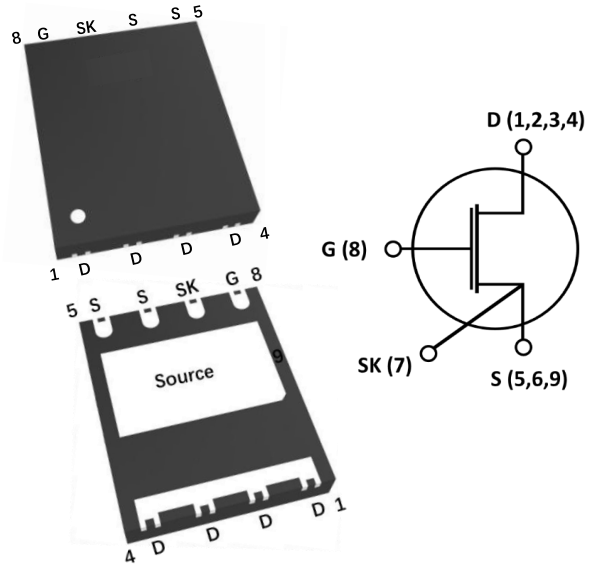
6516EF1

650 V E-mode GaN Transistor



Features

- 650 V enhancement mode GaN power transistor
- GaN-on-Si technology
- DFN 5x6 package
- Typical $R_{DS(on)}$ = 165 mΩ
- $I_{DS\ max,DC}$ = 10 A
- Simple gate drive 0 V to 6 V
- High switching frequency (> 1 MHz)
- Reverse conduction capability
- Zero reverse recovery loss
- Kelvin Source for optimized gate drive

Applications

- PD chargers
- Power Adapters
- Power Factor Correctors
- High density power conversion
- High efficiency power conversion

Description

The 6516EF1 is an enhancement mode GaN transistor designed for large power density and high switching frequency. The excellent properties of GaN enable high-frequency switching at high currents and voltages, leading to high efficiency and reliable power switching.

Pin Description

Pin No.	Pin Name	Description
1,2,3,4	D	Drain
5,6,9	S	Source
7	SK	Kelvin Source
8	G	Gate

Absolute Maximum Ratings

T_J = 25 °C except as noted. Exceeding the maximum ratings may damage the device.

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage – transient (Note 1)	V_{DS} (transient)	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage – transient (Note 1)	V_{GS} (transient)	-20 to 10	V
Continuous Drain Current (T_{case} = 25 °C)	I_{DS}	10	A
Pulsed Drain Current (T_{case} = 25 °C) (Pulse width 10us, V_{GS} = 6 V) (Note 2)	$I_{DS, Pulse}$	17	A
Pulsed Drain Current (T_{case} = 150 °C) (Pulse width 10us, V_{GS} = 6 V) (Note 2)	$I_{DS, Pulse}$	7.5	A
Power Dissipation	P_{tot}	98	W
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C

Note 1: for pulses ≤ 100us

Note 2: Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-to-Case – (bottom side)	$R_{TH,J-C}$	1.27	°C/W
Thermal Resistance Junction-to-ambient (Note 3)	$R_{TH,J-A}$	35.8	°C/W

Note 3: Based on a 4-layer, 1.6 mm-thick PCB. The copper thickness of the external layer is 2 oz. while the buried layers are 1 oz. thick. PCB in a horizontal position without air stream cooling.

Electrical Characteristics

Static Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Condition
Drain-to-Source On Resistance	$R_{DS(on)}$	-	165	260	mΩ	I_{DS} = 3.5 A, V_{GS} = 6 V, T_J = 25 °C
		-	370	-	mΩ	I_{DS} = 3.5 A, V_{GS} = 6 V, T_J = 150 °C
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	1.1	1.6	2.6	V	I_{DS} = 5.25 mA, T_J = 25 °C
		-	1.5	-	V	I_{DS} = 5.25 mA, T_J = 150 °C
Gate-to-Source Current	I_{GS}	-	225	-	µA	V_{GS} = 6 V, T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}	-	1	50	µA	V_{DS} = 650 V, T_J = 25 °C
		-	10	-	µA	V_{DS} = 650 V, T_J = 150 °C
Internal Gate Resistance	R_G	-	1.6	-	Ω	f = 5 MHz; open drain

Dynamic Characteristics

Input Capacitance	C_{ISS}	-	83	-	pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 kHz
Output Capacitance	C_{OSS}	-	34	-	pF	
Reverse Transfer Capacitance	C_{RSS}	-	0.3	-	pF	
Effective Output Capacitance, Energy-Related (Note 4)	$C_{O(ER)}$	-	46	-	pF	V_{DS} = 0 V to 400 V, V_{GS} = 0 V
Effective Output Capacitance, Time-Related (Note 5)	$C_{O(TR)}$	-	61.2	-	pF	
Output Charge	Q_{OSS}	-	24.5	-	nC	V_{DS} = 0 V to 400 V
Turn-On Delay	$t_{D(on)}$	-	3.5	-	ns	V_{DD} = 400 V, V_{GS} = 0 to 6 V, I_{DS} = 6 A, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2.2 Ω (see Figures 14, 15)
Rise Time	t_R	-	6.8	-	ns	
Turn-Off Delay	$t_{D(off)}$	-	2.1	-	ns	
Fall Time	t_F	-	5	-	ns	

Switching Energy during Turn-on	E_{on}	-	16.8	-	µJ	
Switching Energy during Turn-off	E_{off}	-	7.2	-	µJ	
Output Capacitance Stored Energy	E_{OSS}	-	3.7	-	µJ	V_{DS} = 400 V

Note 4: $C_{O(ER)}$ is a fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Note 5: $C_{O(TR)}$ is a fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Gate Charge Characteristics

Total Gate Charge	Q_G	-	2.21	-	nC	V_{GS} = 0 to 6 V, V_{DS} = 0 to 400 V, I_{DS} = 5 A
Gate-to-Source Charge	Q_{GS}	-	0.72	-	nC	
Gate-to-Drain Charge	Q_{GD}	-	0.28	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.11	-	V	V_{DS} = 400 V, I_{DS} = 5 A

Reverse Conduction Characteristics

Source-Drain Reverse Voltage	V_{SD}	-	2.4	-	V	V_{GS} = 0 V, I_{SD} = 2 A
Reverse Recovery Charge	Q_{rr}	-	0	-	nC	
Reverse Recovery Time	t_{rr}	-	0	-	ns	

Electrical Performance Graphs

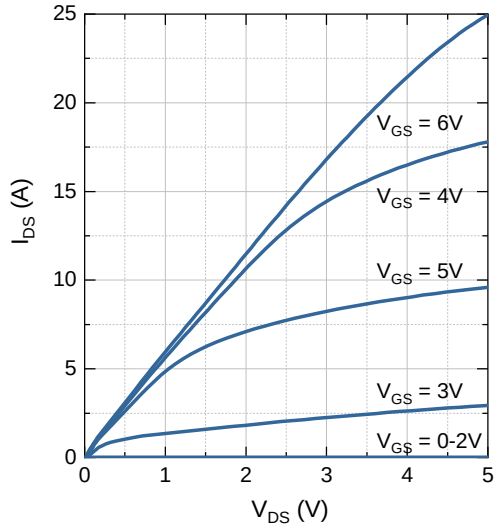


Figure 1: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 25 ˚C

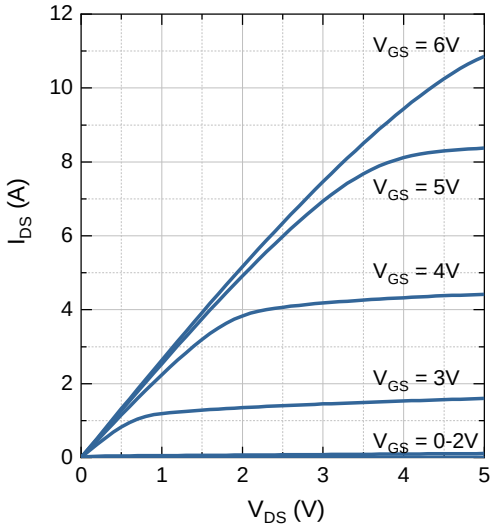


Figure 2: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 150 ˚C

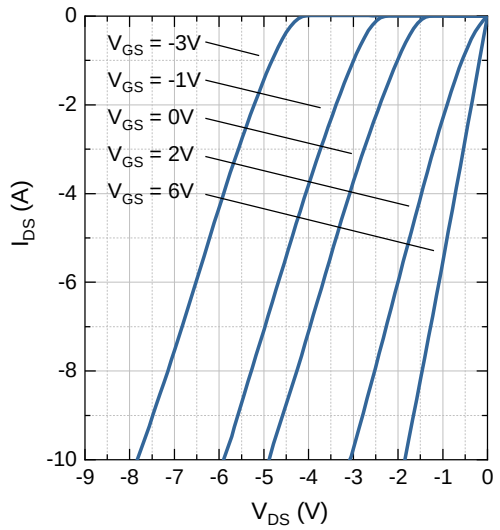


Figure 3: Typical Reverse Conduction Characteristics at T_j = 25 ˚C

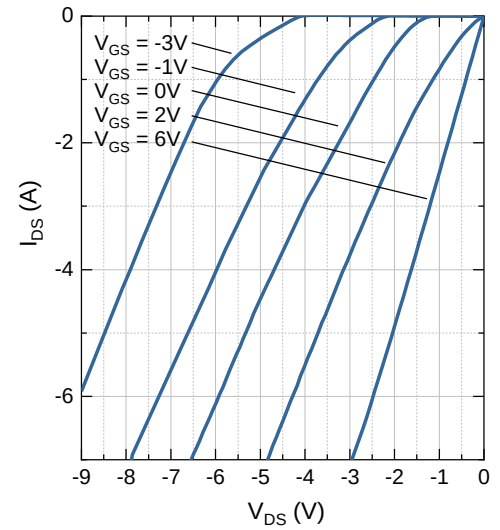


Figure 4: Typical Reverse Conduction Characteristics at T_j = 150 ˚C

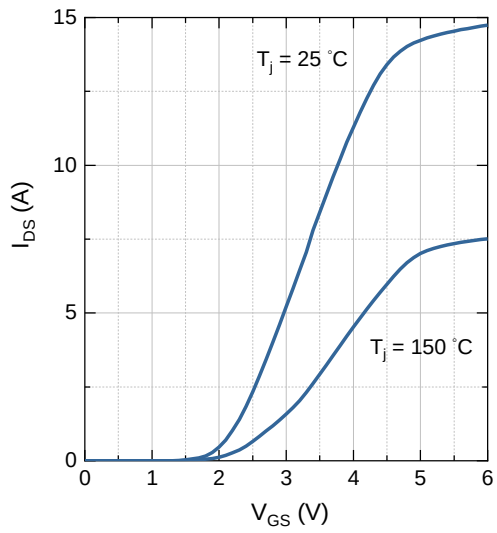


Figure 5: Typical I_{DS} vs. V_{GS} at T_J = 25 °C and T_J = 150 °C for V_{DS} = 3 V

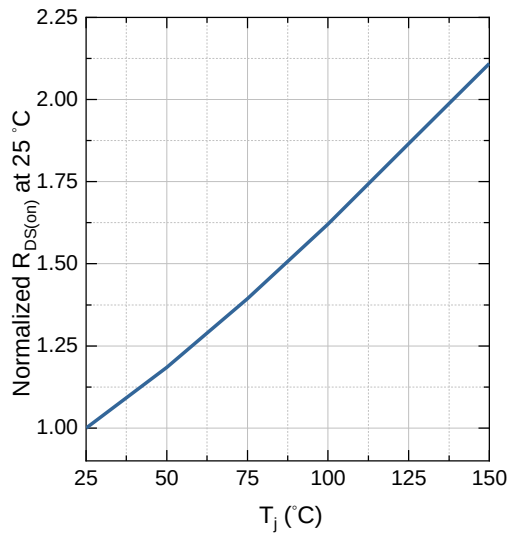


Figure 6: Normalized $R_{DS(on)}$ as a function of T_J

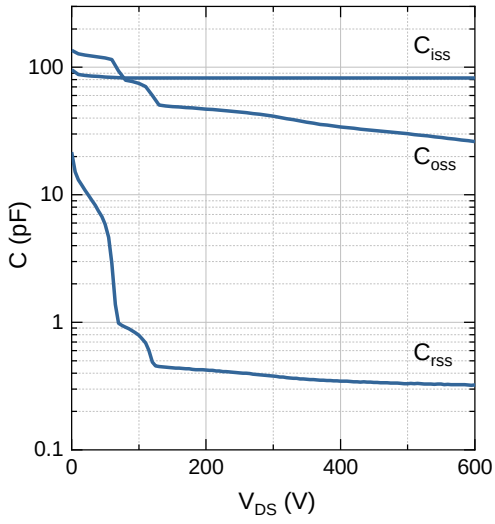


Figure 7: Typical C_{iss}, C_{oss}, C_{rss} vs. V_{DS}

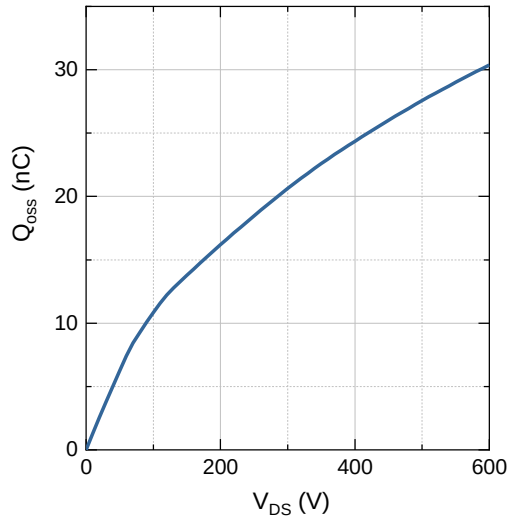


Figure 8: Typical charge stored in C_{oss}

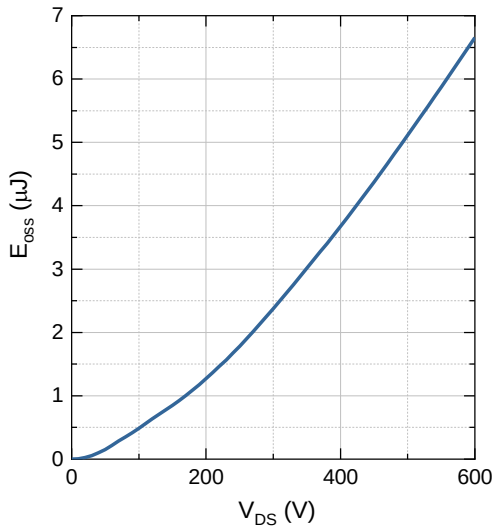


Figure 9: Typical energy stored in C_{oss}

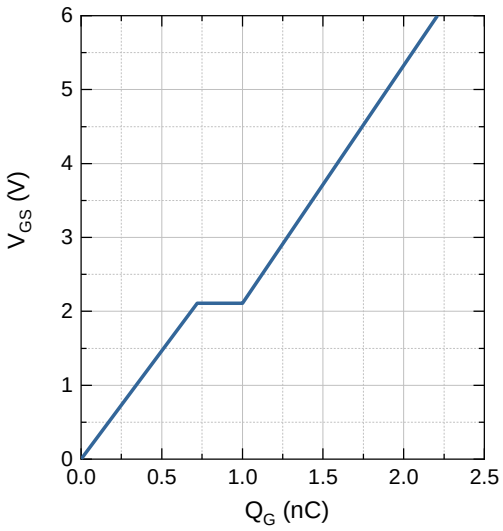


Figure 10: Typical V_{GS} vs. Q_G at V_{DS} = 400 V

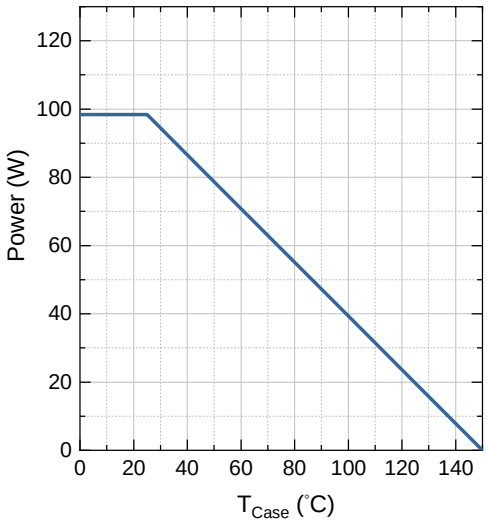


Figure 11: Power Derating vs. T_{case}

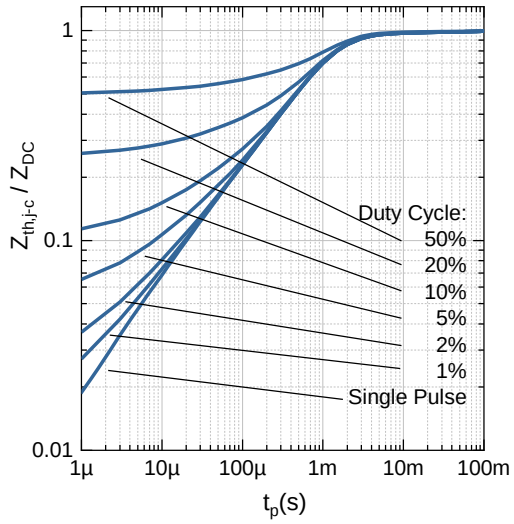


Figure 12: Transient Thermal Impedance

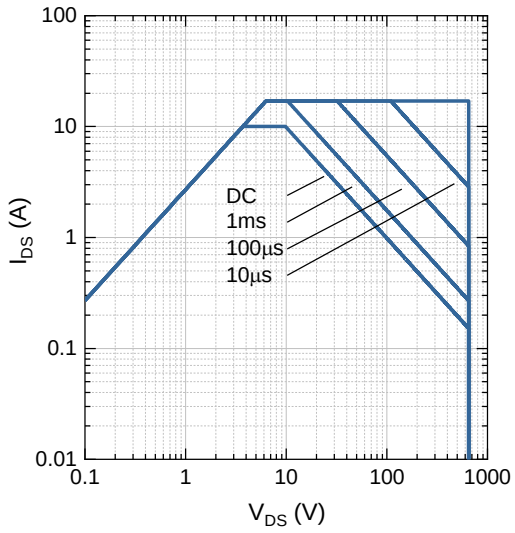


Figure 13: Safe Operating Area at T_{case} = 25 °C

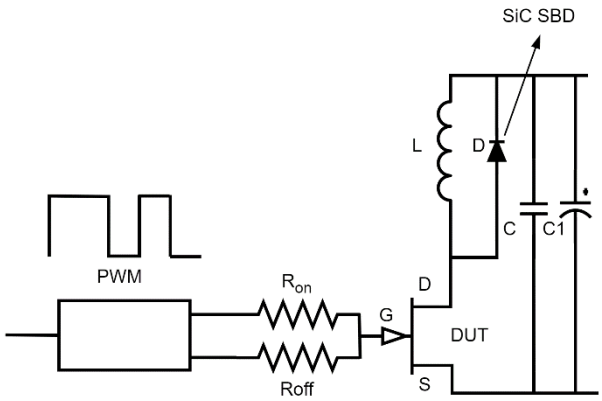


Figure 14: DPT circuit used for switching times measurement, V_{DS} = 400 V, I_{DS} = 6 A, L = 400 µH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 2.2 Ω

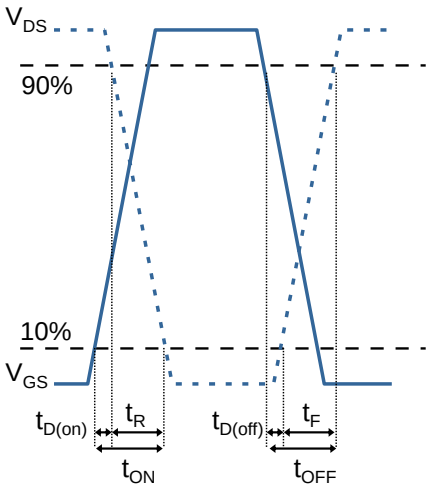
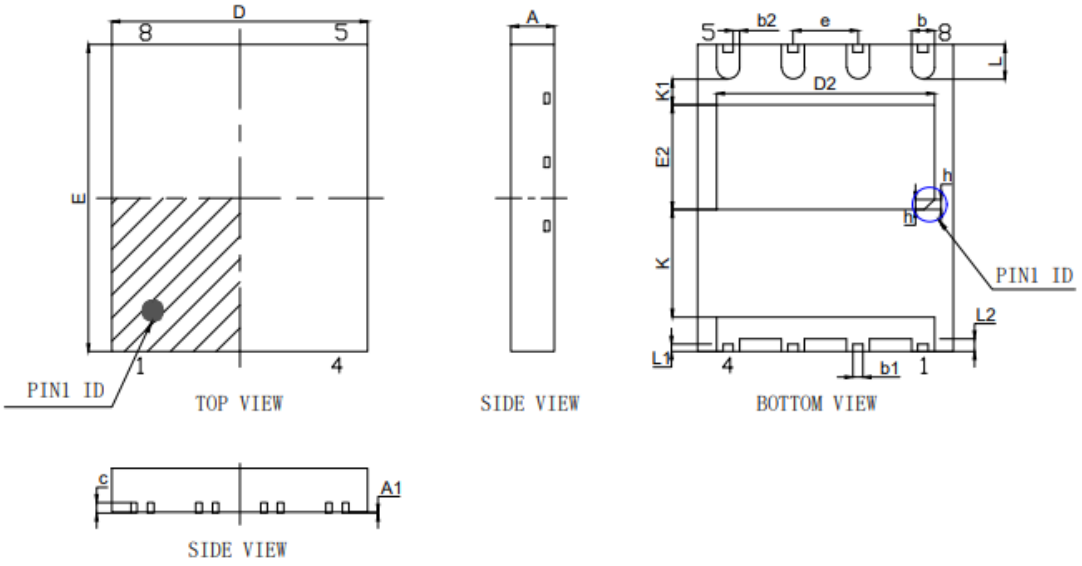


Figure 15: Typical Switching times waveform

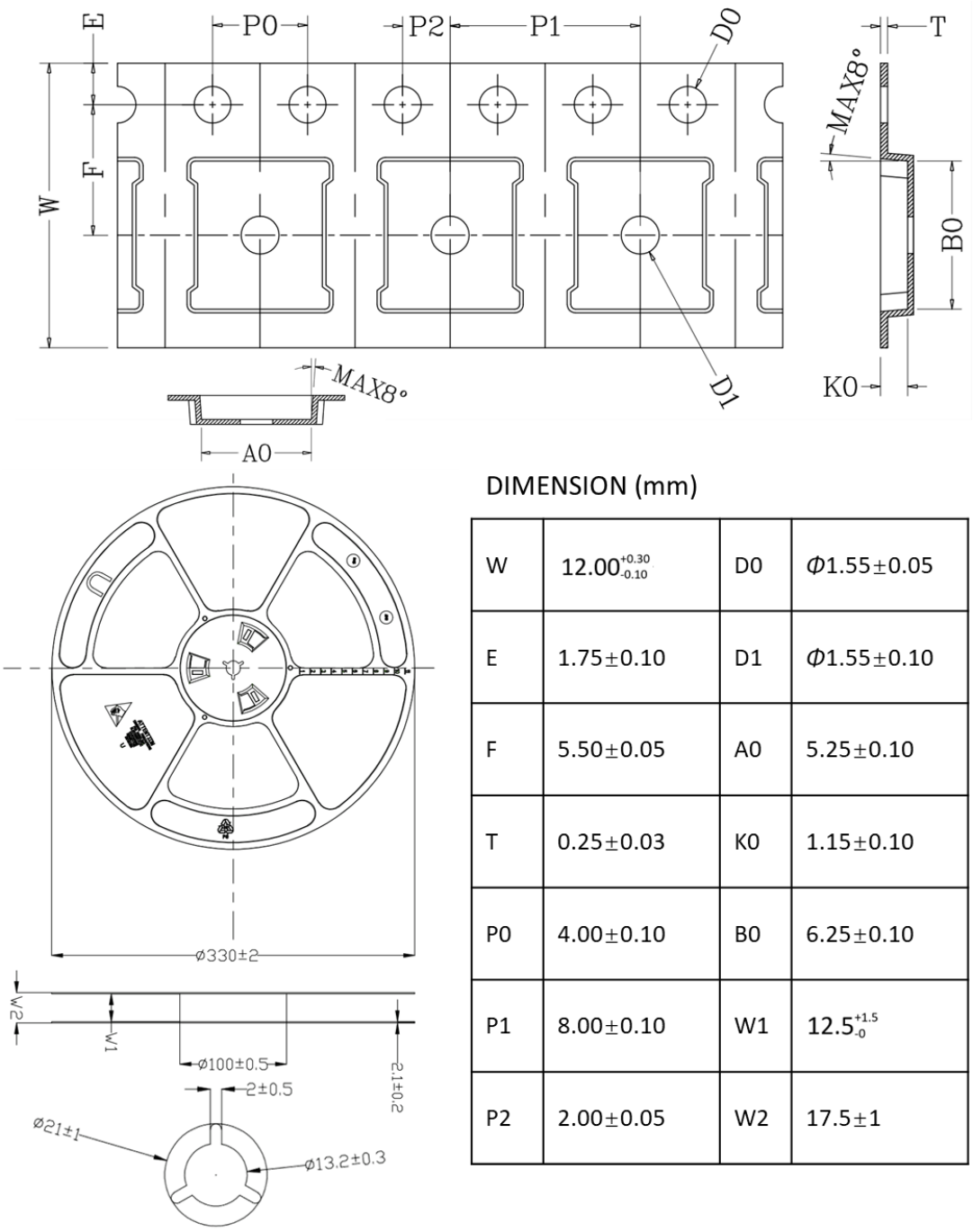
Package Information



SYMBLE	MILLIMETER			SYMBLE	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.85	0.90	E	5.90	6.00	6.10
A1	0	0.02	0.05	E2	1.95	2.05	2.15
b	0.40	0.45	0.50	L	0.625	0.675	0.725
b1	0.20REF			L1	0.15REF		
b2	0.125REF			L2	0.25REF		
c	0.203REF			K	2.10REF		
D	4.90	5.00	5.10	K1	0.50REF		
D2	4.16	4.26	4.36	h	0.15	0.20	0.25
e	1.27BSC						

Notes:
(1)Dimension and tolerance conform to ASME Y14.5-2009.
(2)All dimensions are in millimeters.
(3)Lead coplanarity shall be 0.1 millimeters max.
(4)Complies with JEDEC MO-229.
(5)Drawing is not to scale.
(6)Dimensions do not include mold protrusion.
(7)Package outline exclusive of metal burr dimensions.

Reel Information



DIMENSION (mm)

W	$12.00^{+0.30}_{-0.10}$	D0	Φ1.55±0.05
E	1.75±0.10	D1	Φ1.55±0.10
F	5.50±0.05	A0	5.25±0.10
T	0.25±0.03	K0	1.15±0.10
P0	4.00±0.10	B0	6.25±0.10
P1	8.00±0.10	W1	$12.5^{+1.5}_{-0}$
P2	2.00±0.05	W2	17.5±1

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